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10/527,098	03/09/2005	Rob Anne Beuker	NL02 0815 US	3804

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EXAMINER	
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ART UNIT	PAPER NUMBER
2628	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/527,098	BEUKER, ROB ANNE	
	Examiner	Art Unit	
	TIZE MA	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/25/2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7,9 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7,9,10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 5 of Remarks/Arguments, filed 8/25/2008, with respect to Claim Objections, have been fully considered and are persuasive. The objections to the claims have been withdrawn.

2. Applicant's arguments, see page 5 of Remarks/Arguments, filed 8/25/2008, with respect to Claim rejections under 35 U.S.C. 101, have been fully considered and are persuasive. The rejections of claims have been withdrawn.

3. Applicant's arguments, see pages 5-8 of Remarks/Arguments, filed 8/25/2008, with respect to Claim rejections under 35 U.S.C. 103, have been fully considered but they are not persuasive.

4. Regarding claim 1, the applicant argues: (1) Hashimoto fails to teach "a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers from a block of line pointers in address table register means with the output of pixel counting means" as recited in amended claim 1. Hashimoto teaches a random access mode for writing or reading of a memory circuit (14), see Fig. 3 and column 4 lines 8-11. In the random access mode as taught by Hashimoto, a location in a memory array is accessed by supplying an address that corresponds to the memory location, see column 4 lines 14-17. However, Hashimoto does not teach that in the random access mode data addresses are generated by combining line pointers with pixel count. (2) Hashimoto also fails to teach "a second mode wherein a block of line pointers from a full table of line pointers in said memory is

downloaded into said address table register means" as recited in amended claim 1. In the serial access mode as taught by Hashimoto, data is read out from a memory in the same order in which it is stored into the memory, see column 4 lines 11-14. However, Hashimoto does not teach that in the serial access mode line pointers are downloaded.

5. The examiner disagrees. With respect to the point (1), the memory addresses are generated for memory access, i.e., reading and writing. The scheme of address generation may vary. As long as the modes of access are equivalent, the schemes of generations are considered similar. Although Hashimoto does not teach that in the random access mode data addresses are generated by combining line pointers with pixel count, the random access mode in Hashimoto provides the similar access mode as in the instant claim. Therefore they are considered as similar, or equivalent. In addition, array and table are equivalent. With respect to point (2), the term “download” is treated as read or write since the action is performed between two memory components in the same device. Therefore download is just a memory access. Downloading a block of pointers is the same as serial access of a memory, or reading an array. In summary, the two modes in the instant claim 1 are equivalent to the random access mode and the serial access mode in Hashimoto. The combination of Hashimoto and Hackett renders claim 1 obvious to one of ordinary skill in the art at the time of the invention. Claim 1 remains rejected.

6. Claim 2 remains rejected based on the same rationale as claim 1 above.

7. Claims 4, 5, 7 also remain rejected based on the same rationale as claim 1 above.

8. The newly added claims 9-10 are rejected based on the same rationale as claim 1 above.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-2, 4-5, 7, 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al (US 5,587,962), and in view of Hackett et al (US 5,585,863).

11. Regarding claim 1, Hashimoto et al teaches a method of operating a driving circuit for a display system (Fig. 2 and column 3, line 61—column 4, line 4. memory circuit; frame of pixels) , wherein the sequence of writing and/or reading video data into and/or from a memory is controlled by means of an address sequencer (address sequencers 40a and 40b in Fig. 2), each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line (address generators 28a and 28b in Fig. 2) , the method comprising: operating the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers from line pointers in address table register means with the output of pixel counting means, and in a second mode wherein line pointers from a full table of line pointers in said memory is downloaded into said address table

register means (Fig. 3 and column 4, lines 8-11. Two modes of operations, the random access mode and the serial mode. The random access mode is equivalent to the first mode in the instant claim, and the serial mode is equivalent to the second mode).

12. However, Hashimoto et al generates the memory addresses of the line pointers for the entire frame. That is, Hashimoto et al does not teach the operations based on a block of line pointers.

13. Hackett et al, in the same field of endeavor, teaches creating a line pointer table for a block of lines (column 2, lines 63-66; column 3, lines 15-20. Horizontally dividing the image into rectangular zones of pixel regions is the same as dividing a frame into blocks of lines) for the related pixel regions of a particular interest. This may also saves memory resources.

14. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method as shown in Hashimoto et al by creating a line pointer table for a block of lines as shown in Hackett et al so that the memory address generations and the memory access modes are based on a block of line pointers for the benefit of saving resources.

15. Regarding claim 2, Hashimoto et al teaches a driving circuit for a display system (Fig. 2 and column 3, line 61—column 4, line 4. memory circuit; frame of pixels) comprising a memory for video data to be displayed (memory 24 in Fig. 2) and coupled thereto an address sequencer for controlling the sequence of writing and/or reading the video data in said memory (address sequencers 40a and 40b in Fig. 2), characterized in that the memory contains a full table of line pointers, each line pointer being part of a

memory address for video data, and in that the address sequencer is provided with address table register means for line pointers from said table of line pointers, and pixel counting means (address generators 28a and 28b, address sequencers 40a and 40b in Fig. 2. As seen in column 6, lines 59-62, although Hashimoto does not directly count pixels, the memory address generated has a direct relation with the location of the pixel, by presetting the beginning address. The size of a pixel is known, usually 4 bits.), the output of which in combination with the consecutive line pointers from the address table register means determines the addresses for said video data (Fig. 3 and column 4, lines 8-11. The random access mode); and switching means, by which alternately memory addresses for video data are generated in a first mode in the address sequencer, and in a second mode the address table register is updated with a next block of line pointers (column 4, lines 8-18. Serial access mode and random access mode).

16. However, Hashimoto et al does not teach address table register means for a block of line pointers from said table of line pointers and means for successively updating the address table register means with subsequent blocks of line pointers.

17. Hackett et al, in the same field of endeavor, teaches address table register means for a block of line pointers from said table of line pointers and means for successively updating the address table register means with subsequent blocks of line pointers (column 2, lines 63-66; column 3, lines 15-31. Horizontally dividing the image into rectangular zones of pixel regions is the same as dividing a frame into blocks of lines. Also see that the pointer in one table is used to locate other tables) for the related pixel regions of a particular interest. This may also saves memory resources.

18. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit as shown in Hashimoto et al by creating a line pointer table for a block of lines as shown in Hackett et al so that the memory address generations and the memory access modes are based on a block of line pointers for the benefit of saving resources.

19. Regarding claim 4, Hashimoto et al teaches that the memory comprises a full table of line pointers for different sequences of video data to be displayed (column 5, lines 50-52. Writing addresses generated by the address generator into memory).

20. Claim 5 is rejected based on the same reason as to claim 2 since the driving circuit for display system is always connected to a display system if it is operational.

21. Claim 7 is rejected based on the same reason as to claim 2 since they are the software implementation which is necessary to make the circuit in claim 2 operational.

22. Regarding claim 9, Hashimoto et al teaches a driving circuit for a display system comprising:

a memory (Fig. 2, 24) for video data to be displayed and coupled thereto an address sequence for controlling the sequence of writing and/or reading the video data in said memory (address generators 28a and 28b, address sequencers 40a and 40b in Fig. 2.)

means for successively updating the address table register means with subsequent line pointers (column 4, lines 8-18. Serial access mode); and

pixel counting means, the output of which in combination with the consecutive line pointers from the address table register means determines the addresses for said video data (address generators 28a and 28b, address sequencers 40a and 40b in Fig. 2. As

seen in column 6, lines 59-62, although Hashimoto does not directly count pixels, the memory address generated has a direct relation with the location of the pixel, by presetting the beginning address. The size of a pixel is known, usually 4 bits.)

23. However, Hashimoto et al does not teach address table register means for a block of line pointers.

24. Hackett et al, in the same field of endeavor, teaches address table register means for a block of line pointers (column 2, lines 63-66; column 3, lines 15-31. Horizontally dividing the image into rectangular zones of pixel regions is the same as dividing a frame into blocks of lines. Also see that the pointer in one table is used to locate other tables) for the related pixel regions of a particular interest. This may also saves memory resources.

25. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit as shown in Hashimoto et al by creating a line pointer table for a block of lines as shown in Hackett et al so that the memory address generations and the memory access modes are based on a block of line pointers for the benefit of saving resources.

26. Claim 10 is rejected based on the same reason as to claim 5 since they are the software implementation which is necessary to make the circuit in claim 5 operational.

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TIZE MA whose telephone number is (571)270-3709. The examiner can normally be reached on Mon-Fri 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao M. Wu can be reached on 571-272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tm

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